UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,612	07/17/2003	Eric T. Stubbs	M4065.0322/P322-A	9666

24998 7590 10/11/2005		EXAMINER
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP		ANDERSON, MATTHEW D
2101 L Street, NW		
Washington, DC 20037	ART UNIT	PAPER NUMBER
	2186	

DATE MAILED: 10/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

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	Application No.	Applicant(s)
Office Action Summary	10/620,612	STUBBS ET AL.
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>20 September 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>34-44 and 53-56</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>34-44 and 53-56</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>17 July 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 34-40 and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Dell et al. (US Patent # 6,092,146) and Bosnyak (US Patent # 4,625,162).

3.   With respect to claim 34, Dell et al. disclose:

a signaling circuit for encoding presence detect data comprising: a first signal encoding

portion for encoding first presence detect information, said first presence detect information

being disposed in a hard-wired circuit of an integrated circuit semiconductor memory device

(figure 1, item 100) during the manufacturing of said integrated semiconductor memory device,

said hard-wired circuit formed during manufacturing of said semiconductor memory device, by

teaching in Table 1 in column 6 of serial presence detect (SPD) data being factory set;

and a second signal encoding portion for encoding second presence detect information

said second information being disposed in a programmable circuit of said semiconductor

memory device, said programmable circuit programmed subsequent to manufacturing of said

semiconductor memory device, by teaching in Table 1 and the subsequent tables indicated

therein for the programming of particular SPD bytes.

4.   With respect to claim 35, Dell et al. disclose data relating to a storage capacity of said semiconductor memory device, as shown in Table 3.2 in column 7.

5.   With respect to claim 36, Dell et al. disclose data relating to a data bus width of said semiconductor memory device, as shown by the data width sizes in Table 2.1.

6.   With respect to claim 37, Dell et al. disclose data relating to a data access speed of said semiconductor memory device, as shown in Table 4.2 in column 7.

7.   With respect to claim 38, Dell et al. disclose data relating to a column address strobe latency of said semiconductor memory device, as shown in Table 3.2 in column 7.

8.   With respect to claim 39, Dell et al. disclose data relating to a data refresh rate of said semiconductor memory device, as discussed in column 5, lines 60+.

9.   With respect to claim 40, Dell et al. disclose data relating to an interface voltage of said semiconductor memory device, as discussed in column 6, lines 5+.

10.   With respect to claim 53, Dell et al. disclose:

receiving a first signal at a memory controller from said memory integrated circuit (figure 1, item 100), said first signal encoding first presence detect information hardwired into said memory integrated circuit during manufacturing of said memory integrated circuit, by teaching in Table 1 in column 6 of serial presence detect (SPD) data being factory set;

and receiving a second signal at a memory controller from said memory integrated circuit, said second signal encoding second presence detect information programmed into said memory integrated circuit subsequent to manufacturing of said memory integrated circuit, by teaching in Table 1 and the subsequent tables indicated therein for the programming of particular SPD bytes.

11.   With respect to claim 54, Dell et al. disclose receiving a control signal at said memory

integrated circuit from said memory controller, said control signal being related to at least one of

said first signal and said second signal, as shown in figure 4.

12.   With respect to claim 55, Dell et al. disclose receiving an address signal at said memory

integrated circuit from said memory controller, said address signal having a format related to at

least one of said first signal and said second signal, as shown by the RAS and CAS signals in

figure 4.

13.   With respect to claim 56, Dell et al. disclose recognizing an identity of said memory

integrated circuit at said memory controller based on said first and second signals, by teaching in

Table 1 of using the SPD bytes to determine the memory type or configuration type.

14.   With respect to independent claims 34 and 53, Dell teaches all other limitations as

discussed above, but fails to specifically disclose said first presence detect data having one of a

first value associated with a short circuit within said hardwired circuit and a second value

associated with an open circuit within said hardwired circuit. Bosnyak teaches in column 1, lines

24-30, that array bits are set to one of two logical states by either keeping the fuse for that bits

intact (short circuit), or blowing the fuse to create and open circuit.

15.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Dell et al. and Bosnyak before him at the time the invention was made, to modify the factory

setting taught by Dell et al., to instead be hardwired as in the conventional art of Bosnyak, in

order to provide static settings, as taught by Bosnyak.

16.   Claims 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al.

and Bosnyak.

17.   With respect to claims 41, Dell et al. and Bosnyak teach all other limitations as discussed

above, including wherein said first signal portion and said second signal portion comprise first

and second serial data signals respectively, as shown in Table 1, but does not specifically

disclose said first and second serial data signals being adapted to be transmitted over a single

data line.

18.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Dell *et al.* and Bosnyak before him at the time the invention was made, to modify the presence

detect bits taught by Dell *et al.*, to be sent over a single data line in order to conserve chip space,

as well known in the art.

19.   With respect to claims 42-44, the difference between Dell *et al.* and Bosnyak and the

claims is the claims recite the circuit being a fuse device, antifuse device, or a transistor-based

device. However, the specific use of these particular device types does not have a disclosed

purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would

have been an obvious matter to one skilled in the art to utilize the circuitry of Dell *et al.* and

Bosnyak with any of these types of devices in order to gain their benefits, since applicant has not

disclosed that a particular device type, as opposed to other memory devices, overcomes a

deficiency in the prior art or is for any stated purpose.

20.   Claims 34-44 and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Dell et al. and Bosnyak.

21.   In addition to that discussed above, with respect to claims 34 and 53, assuming arguendo,

the difference between Dell *et al.* and Bosnyak and the claims is the claims recite the presence

detect data being stored on an integrated semiconductor memory device. However, the specific

use of an integrated device does not have a disclosed purpose nor are disclosed to overcome any

deficiencies in the prior art. Accordingly, it would have been an obvious matter to one skilled in

the art to utilize the circuitry of Dell *et al.* and Bosnyak as an integrated semiconductor device,

since applicant has not disclosed that a particular device type, as opposed to other memory

devices, overcomes a deficiency in the prior art or is for any stated purpose. See also MPEP

2144.04 as to why making elements integral would be merely a matter of obvious engineering

choice.

22.   Claims 34-44 and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Dell et al., Bosnyak, and Gowda et al. (US Patent # 6,275,259).

23.   In addition to that discussed above, with respect to claims 34 and 53, assuming arguendo,

the difference between Dell *et al.* and Bosnyak and the claims is the claims recite the first

presence detect data being hardwired instead of factory set, as disclosed in Dell et al.. Gowda et

al. though teaches in column 4, lines 28-34, that the factory setting of the present invention

allows for the use of algorithms implemented in digital circuitry for the automatic gain control

function.

24.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Dell *et al.*, Bosnyak, and Gowda *et al.* before him at the time the invention was made, to modify

the factory setting taught by Dell *et al.* and Bosnyak, to instead be hardwired as in the

conventional art of Gowda *et al.*, in order to provide static settings, as taught by Gowda *et al.*.

Response to Arguments

25.   Applicant's arguments filed 9/20/05 have been fully considered but they are not

persuasive.

26.   Applicants' attempts to define "hardwired" as not programmable are not supported by the

27.   specification. The hardwired presence detect bits in page 10, lines 28-29 correspond to

those in lines 23-24, which clearly states that those presence detect bits are programmed.

Therefore, it is clear that the claimed "hardwired" does NOT mean that the bits are not

programmed, and will not be interpreted as such. Because "hardwired" is not limited to bits that

are not programmed, the factory set bits in Dell are considered to be hardwired.

Conclusion

28.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Matthew D. Anderson whose telephone number is (571) 272-

4177. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew D. Anderson
Primary Examiner
Art Unit 2186